IN THE CLAIMS:

Please cancel claims 4, 6 and 14 without prejudice or disclaimer, amend claims 1-3, 6, 7, 13, 17, 20-22, 30, 31, 33-37 and 39, and add new claims 41-45 as follows:

1. (Currently Amended) A semiconductor device comprising a plurality of signal terminals of a circuit block,

wherein the signal terminals are arranged within a frame of the circuit block and along a second direction that intersects ~~an extending~~ a first direction [[of]] along which a plurality of wirings extend, ~~which is a~~ the wirings are wirings of an upper layer and outside the circuit block, and the wirings are connected to the signal terminals via a plurality of through holes, [[and]]

wherein each of the signal terminals ~~is arranged~~ extends in the second direction ~~that intersects the extending direction outside the circuit block~~ so that ~~spaces for a plurality of wiring channels can be secured~~ a dimension thereof in the second direction passes through at least two of the plurality of wirings.

2. (Currently Amended) The semiconductor device according to claim 1, wherein a plurality of the circuit blocks are arranged along the [[extending]] first direction of the wiring outside the circuit blocks, and the signal terminals of each of the circuit blocks and the wiring outside the circuit blocks are electrically connected to each other.

3. (Currently Amended) The semiconductor device according to claim 2, wherein a wiring area is provided between a group of ~~different~~ circuit blocks among the circuit blocks.

4. (Cancelled)

5. (Withdrawn) The semiconductor device according to claim 1, wherein the plurality of the signal terminals are arranged along the extending direction of the outside-cell wiring and the position of the terminals for mutually adjoining signals along the extending direction of the outside-cell wiring are shifted to the direction that intersects the extending direction of the outside-cell wiring.

6. (Cancelled)

7. (Currently Amended) The semiconductor device according to claim 1, wherein the signal terminals are [[is]] constituted of a top wiring layer in the circuit block.

8. (Withdrawn) The semiconductor device according to claim 1, wherein a power supply terminal that extends to the direction that intersects the extending direction of the wiring outside the circuit block is provided in the frame of the circuit block.

9. (Withdrawn) The semiconductor device according to claim 8, the power supply terminal is constituted of a top wiring layer in the circuit block.

10. (Withdrawn) A semiconductor device, wherein a power supply terminal of a circuit block is extended to the direction that intersects the extending direction of power supply wiring that is wiring of the upper layer and is connected to the power supply terminal, then extends the upper part of the circuit block.

11. (Withdrawn) The semiconductor device according to claim 10, wherein the power supply terminal is extended from end to end in the frame of the circuit block.

12. (Withdrawn) The semiconductor device according to claim 10, wherein the power supply terminal is constituted of the top wiring layer in the circuit block.

13. (Currently Amended) A semiconductor device, comprising:

a plurality of circuit blocks arranged along a first direction; and

~~a first~~ wirings that extend[[s to]] in the first direction and electrically connects between the plurality of circuit blocks,

wherein a plurality of signal terminals are arranged in a frame of each of the plurality of circuit blocks and along a second direction that intersects the first direction;

wherein each of the plurality of signal terminals ~~secures spaces for a plurality of wiring channels~~ extends in the second direction so that a dimension thereof in the second direction passes through at least two of the wirings; and

wherein the ~~first~~ wirings are arranged on ~~the wiring layer of the~~ an upper layer [[is]] outside the circuit block and are electrically connected to ~~each of~~ the plurality of signal terminals via a plurality of through holes.

14. (Cancelled)

15. (Withdrawn) The semiconductor device according to claim 13, wherein a plurality of each of the plurality of signal terminals are arranged along the first direction and the signal terminals that are mutually adjacent to the first direction are arranged, shifting the position to the second direction.

16. (Withdrawn) The semiconductor device according to claim 13, wherein each of the plurality of signal terminals is arranged in the frame of the circuit block.

17. (Currently Amended) The semiconductor device according to claim 13, wherein each of the plurality of signal terminals is constituted of [[the]] a top wiring layer in the circuit block.

18. (Withdrawn) The semiconductor device according to claim 13, wherein a power supply terminal that extends to the second direction is provided in the frame of the circuit block.

19. (Withdrawn) The semiconductor device according to claim 18, wherein the power supply terminal is constituted of the top wiring layer in the circuit block.

20. (Currently Amended) The semiconductor device according to claim 13, wherein one of the circuit blocks is a memory circuit, one of the ~~first~~ wirings constructs a wiring for an address signal, and said one of the ~~first~~ wirings is connected in common to said one of the circuit blocks.

21. (Currently Amended) The semiconductor device according to claim 13, wherein one of the circuit blocks is a memory circuit, one of the ~~first~~ wirings is wiring for data input, and t said one of the ~~first~~ wirings is connected in common to said one of the

circuit blocks.

22. (Currently Amended) The semiconductor device according to claim 13, wherein one of the circuit blocks is connected to a wiring for a different clock signal.

23. (Withdrawn) The semiconductor device according to claim 1, wherein the circuit block is a memory circuit and the signal terminal is formed on an input/output circuit area of the memory circuit.

24. (Withdrawn) A manufacturing method of a semiconductor device, comprising the steps of:

(a) arranging a plurality of circuit blocks along a first direction; and

(b) electrically connecting between the plurality of circuit blocks using first wiring that extends to the first direction,

wherein a plurality of signal terminals are arranged in each of the plurality of circuit blocks along a second direction that intersects the first direction;

wherein spaces for a plurality of wiring channels are secured in the second direction in each of the plurality of signal terminals; and

wherein the first wiring is arranged on the wiring layer of the upper layer than the signal terminal and electrically connected to the signal terminal.

25. (Withdrawn) A storage medium that stores data for designing an integrated circuit to be formed on a semiconductor chip,

wherein the data stored in the storage medium has data of a plurality of circuit blocks arranged along a first direction and first wiring data that extends to the first direction and electrically connects between the plurality of circuit blocks;

wherein each of the plurality of circuit blocks has data of a plurality of signal terminals arranged along a second direction that intersects the first direction;

wherein each of the plurality of signal terminals has data in which spaces for a plurality of wiring channels are secured in the second direction; and

wherein data in the connected state between each of the plurality of signal terminals and the first wiring arranged on the wiring layer of the upper layer is provided.

26. (Withdrawn) The storage medium according to claim 25, comprising data arranged in the state in which each of the plurality of signal terminals is extended in the second direction.

27. (Withdrawn) The storage medium according to claim 25, comprising data in which each of the plurality of signal terminals is arranged along the first direction and the signal terminals that are mutually adjacent to the first direction are arranged, shifting the position to the second direction.

28. (Withdrawn) The storage medium according to claim 25, comprising data in which each of the plurality of signal terminals is arranged in the frame of the circuit block.

29. (Withdrawn) The storage medium according to claim 25, wherein a semiconductor integrated circuit is designed using the storage medium.

30. (Currently Amended) The semiconductor device according to claim [[14]]13,

wherein one of the circuit blocks is a memory circuit, and

wherein one of the signal terminals is formed on [[the]] an input/output circuit area of the memory circuit.

31. (Currently Amended) The semiconductor device according to claim 30,

wherein one of the ~~first~~ wirings is a wiring for an address signal or a wiring for data.

32. (Withdrawn) The semiconductor device according to claim 24,

wherein the circuit block is a memory circuit, and

wherein the signal terminal is formed on the input/output circuit area of the memory circuit.

33. (Currently Amended) A semiconductor device, comprising:

a plurality of memory circuits arranged along a first direction; and

a plurality of first wirings ~~that are~~ extending in the first direction and being

electrically connected to the plurality of memory circuits,

wherein a plurality of signal terminals are [[is]] arranged in a frame of each of the plurality of memory circuits and along a second direction that intersects the first direction;

wherein the plurality of first wirings are formed on ~~the wiring layer of the~~ an upper layer outside the circuit block and ~~of the signal terminal~~, and extend over the signal terminals ~~for the signal along the first direction~~;

wherein each of the signal terminals ~~secures spaces for a plurality of wiring channels~~ extends in [[a]] the second direction ~~that intersects the first direction~~ so that a dimension thereof in the second direction passes through at least two of the first wirings; and

wherein ~~each of~~ the plurality of first wirings are [[is]] ~~arranged on a different wiring channel in the plurality of wiring channels and is~~ electrically connected to ~~the terminal for the different signal in~~ the signal terminals ~~of the plurality of memory circuits arranged in the first direction~~ via a plurality of through holes.

34. (Currently Amended) The semiconductor device according to claim 33, comprising:

a second wiring formed on the [[same]] upper layer ~~wiring layer~~ as the first wiring,

wherein the second wiring is electrically connected to each of the signal terminals of the plurality of memory circuits positioned on ~~the same~~ an identical wiring channel.

35. (Currently Amended) The semiconductor device according to claim 33, wherein one of the first wirings is a wiring for an address signal.

36. (Currently Amended) The semiconductor device according to claim 33, wherein one of the first wirings is a wiring for data.

37. (Currently Amended) The semiconductor device according to claim 33, wherein one of the first wirings is a wring for a clock signal.

38. (Withdrawn) The semiconductor device according to claim 33, wherein the signal

terminal is formed on an input/output circuit area of the memory circuit.

39. (Currently Amended) The semiconductor device according to claim 34,

wherein one of the first wirings is ~~one of wirings~~ for [[the]] an address signal and another one of the first wirings is for [[the]] data; and

wherein the second wiring is ~~the other of wirings~~ for [[the]] an address signal [[and]] or for [[the]] data.

40. (Withdrawn) The semiconductor device according to claim 33, wherein in each of the memory circuit, a plurality of the signal terminals are arranged in the first direction and second direction, and the signal terminals adjacent to the first direction are arranged, shifting the position to the second direction.

41. (New) The semiconductor device according to claim 1, wherein the circuit block is a memory circuit, and one of the signal terminals is formed on an input/output circuit area of the memory circuit.

42. (New) The semiconductor device according to claim 41, wherein the memory circuit constitutes a Random Access Memory.

43. (New) The semiconductor device according to claim 20, wherein the memory circuit constitutes a Random Access Memory.

44. (New) The semiconductor device according to claim 21, wherein the memory circuit constitutes a Random Access Memory.

45. (New) The semiconductor device according to claim 39, wherein one of the memory circuits constitutes a Random Access Memory.